Methods and Devices for Digital Video Signal Compression and Multi-Screen Process by Multi-Thread Scaling

TECHNICAL FIELD

The present invention relates to the method and device for digital video signal compression/multi-screen process by multi-thread scaling.

BACKGROUND ART

Compression/multi-screen process of digital video signals may be used in a digital video recorder (DVR) which converts analog images into digital images and records/stores such images, or displays such images real time.

Ordinarily, a DVR must compress and record multi-channel video signals inputted from a number of cameras, and must display such signals on multi-screens.

Among various modules constituting such DVR system, the compression unit and the multi-screen processor are the most important modules. In the conventional multi-channel DVR systems, such compression units and multi-screen processors are set apart as independent modules.

The multi-thread scaling means to process screens of different resolutions alternating the even field and the odd field of interlacing.

Figure 1 is a diagram illustrating a conventional DVR system with an independent compression unit and an independent multi-screen processor.

Operations of the compression unit (10) illustrated in Figure1 are explained herein below. First of all, the central processing unit ("CPU") (13) initializes the analog/digital converters (11), and the compression FIFO (12) in the pre-determined

order. Such initialized analog/digital converters (11) store digital data in the compression FIFO (12) and issues to the CPU (13) an interrupt exception handling request. Although the CPU (13) may fetch video data after polling the analog/digital converters (11), the compression FIFO (12) is used in order to decrease the load on the CPU (13), to increase the video data transmission efficiency, and to reduce transmission errors. The CPU (13)'s exception handling routine transmits video data from the compression FIFO (12) to the memory (RAM) (30) by a direct memory access method, encodes such data using compression algorithms such as MPEG, JPEG, and H.26x, etc., and then stores the data in a storage such as a hard disk.

The multi-screen processor (20) as illustrated in Figure 1 operates as follows. In the multi-screen processor, the video processor (23) transmits digitalized video data from the multi-screen FIFO (22) to the video memory (31) according to the pre-determined rules set for the multi-screen processing. Then, such data are processed to constitute multi-screens, such as 4/8/16 screens, on a TV or a VGA monitor.

As explained above, the conventional system has dependent modules for the compression unit (10) and the multi-screen processor (20) because the compression unit (10) and the multi-screen processor (20) are programmed to process video data in different resolutions. In other words, the compression unit (10) may process video data real time only if it is programmed to be a 30 frame transmission mode at the resolution of 352x240. Also, the multi-screen processor (20) for 16 screens, for example, may process video data real time only if it is programmed to be a 30 frame transmission mode at the resolution of 180x120. Therefore, the conventional N-channel DVR with independent compression unit (10) and multi-screen processor (20) requires 2xN analog/digital converters.

However, ordinary analogy/digital converters consume an extraordinary amount of the current and a great amount of electric power. Accordingly, they generate a significant amount of heat impairing stability of the system. Furthermore, conventional multi-channel DVR systems are expensive because (N channel)x2 analog/digital converters are required.

DISCLOSURE OF THE INVENTION

The present invention has a purpose to, by using the multi-thread scaling to process screens of different resolutions alternately in the even field and the odd field of interlacing, provide the method and device for digital video signal compression/multi-screen process only with N analog/digital converters, which method and device integrates the conventional compression unit and multi-screen processor requiring 2xN analog/digital converters.

In order to accomplish the above-mentioned purpose, the present invention's method to compress and process for multi-screens digital video signals by multi-thread scaling uses a single integrated analog/digital converter for each channel for compression/multi-screen process. The present invention's method comprises: (a) a step to scale the resolutions of digital video signals outputted from analog/digital converters depending on the even/odd fields of the inputted video signals; and (b) a step to compress or process for multi-screens the scaled digital video signals according to the resolutions scaled in the said step (a). The present invention's device for compression and multi-screen process of digital video signals by multi-thread scaling comprises: multi-channel analog/digital converters, which generate even/odd field indicators depending on the fields of the inputted multi-channel video signals and scale

the resolution of each channel's video signals for compression or for multi-screen process while converting such signals into digital signals according to the even/odd fields of the signals; a compression FIFO which stores, for compression, the video signals outputted from each channel's analog/digital converter based upon the even/odd field indicator of such analog/digital converter; a multi-screen FIFO which stores, for multi-screen process, the video signals outputted from each channel's analog/digital converter based upon the even/odd field indicator of such analog/digital converter; a CPU which initializes each channel's analog/digital converter, the compression FIFO, and the multi-screen FIFO, and controls each channel's analog/digital converter so that the converted digital video signals may be scaled into various resolutions depending on the fields of the inputted multi-screen video signals; and a video processor which transmits to the video memory the video signals which were inputted to the said multi-screen FIFO according to the rules pre-determined for the multi-screen process.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will further be described by way of example and with reference to the following drawings, in which,

Figure 1 is a diagram illustrating a conventional DVR system with an independent compression unit and an independent multi-screen processor.

Figure 2 is a flow chart for the compression/multi-screen process method for N channel digital video signals using N analog/digital converters according to the present invention.

Figure 3 is a diagram illustrating, as a preferred embodiment of the present invention, the device for digital video signal compression/multi-screen process

integrating the compression unit and the multi-screen processor.

Figure 4 is a diagram illustrating the operation principle of the multi-thread scaling of the present invention's method and device.

Detailed explanations of a preferred embodiment of the method and device for digital video signal compression/multi-screen process by multi-thread scaling are provided in the following with reference to the attached drawings.

BEST MODE FOR CARRYING OUT THE INVENTION

Figure 2 is a flow chart for the compression/multi-screen process method for N channel digital video signals using N analog/digital converters according to the present invention.

The initialization of auxiliary devices (S100) is a step in which the CPU initializes each channel's analog/digital converter, the compression FIFO, and the multi-screen FIFO.

The generation of even field/odd field indicators (S110) is a step in which the initialized analog/digital converter of each channel generates even field/odd field indicators. Figure 4 illustrates such generated even field/odd field indicators corresponding to time indicated on the time axis.

If the generated even field/odd field indicator is even, the 352x240 scaling (S120) is a step in which outputs digitalized video signals scaled to 352x240, and the said outputted digital video signals are transmitted to the compression FIFO (S130).

If the generated even field/odd field indicator is odd, digitalized video signals scaled to 180x120 for 16 screens, to 240x160 for 9 screens, or to 360x240 for 4 screens, are outputted (S140), and the outputted digital video signals are transmitted to the

multi-screen FIFO (S150). At the step S140, the CPU is programmed to control the operation register of each channel's analog/digital converter so that the video signals may be scaled to 180x120 for 16 screens, to 240x160 for 9 screens, or to 360x240 for 4 screens in the event that the field indicator is odd.

Figure 3 is a diagram illustrating, as a preferred embodiment of the present invention, the device for digital video signal compression/multi-screen process in an N-channel DVR system with N analog/digital converters.

As illustrated in Figure 3, the device has an integrated compression/multi-screen processor (40). In the following, compression of the inputted analog video signals in the even field and multi-screen process, for 4/9/16 multi-screens, of the inputted signals in the odd field are explained.

N analog/digital converters (41), after being initialized by the CPU (44), generate even field/odd field indicators, digitalize each channel's video signals and scale them to the resolutions of 180x120 for 16 screens, 240x160 for 9 screens, 360x240 for 4 screens, or 352x240 for the normal screen. If the even field/odd field indicator is even, the digitalized video signals, which have been scaled to the resolution of 352x240, are stored in the compression FIFO (42). If the even field/odd field indicator is odd, the digitalized video signals, which have been scaled to the resolutions of 180x120 for 16 screens, 240x160 for 9 screens or 360x240 for 4 screens, are stored in the multi-screen FIFO (43).

The compression FIFO (42) stores in it the video signals outputted from each channel's analog/digital converter (41) if the even field/odd field indicator is even. Although the CPU (44) may fetch digitalized video signals after polling the said analog/digital converter group (41), the present invention uses the compression FIFO

(42) in order to reduce the load on the CPU (44), to raise the transmission efficiency of video signals, and to reduce transmission errors.

The multi-screen FIFO(43) stores the scaled video signals outputted from each channel's analog/digital converter if the even field/odd field indicator is odd.

The CPU (44) initializes the analog/digital converter (41) of each channel, the compression FIFO and the multi-screen FIFO. Furthermore, the CPU (44) controls the said analog/digital converters (41) so that the digitalized video signals may be scaled to various resolutions according to the even field/odd field indicators generated at each channel's analog/digital converter. The CPU (44) is programmed to control the operation register of each channel's analog/digital converter (41) so that the video signals may be scaled to the resolutions of 180x120 for 16 screens, 240x160 for 9 screens, or 360x240 for 4 screens in the event that the field indicator is odd.

The video processor (45) transmits to the video memory the video signals which have been inputted to the multi-screen FIFO in accordance with the rules pre-determined for the multi-screen process.

Figure 4 is a diagram illustrating the operation principle of the multi-thread scaling of the present invention.

Figure 4 illustrates even field/odd field indicators generated by each channel's analog/digital converter corresponding to the time represented at the time axis. Based upon such even field/odd field indicators, the CPU (44) controls the operation registers of the analog/digital converters (41) of each channel.

As explained in the foregoing, according to the present invention's method and device for digital video signal compression and multi-screen process by multi-thread scaling, the processor for compression/multi-screen process may conduct the

compression and multi-screen process sequentially from the compression FIFO and the multi-screen FIFO depending on the even/odd fields of the signals. Thus, compared with the conventional multi-channel DVR system which uses 2*N analog/digital converters for N channels, the present invention's method and device uses N analog/digital converters for the same N channels while providing the same function as the conventional system.

By implementing a system equivalent to the conventional system, which requires 2xN ADC, with only N analog/digital converters, the present invention saves the electricity and expense required for the conventional system by 100%. In addition to the effect of saving the electricity consumed for the system, the present invention also increases the stability of the multi-channel DVR system by reducing the number of required analog/digital converters.